

Process Kit For Erosion Resistance Enhancement

FIELD OF THE INVENTION

The present invention generally relates to a process kit surrounding a semiconductor workpiece in a plasma chamber that can improve the spatial uniformity of plasma energy distribution over the workpiece surface. More specifically, the present invention relates to a film of fluorocarbon-based polymer covering the top surface of the process kit that can resist plasma-related erosion, reduce particulate contamination during etching, and prolong the lifetime of the process kit.

BACKGROUND OF THE INVENTION

Semiconductor fabrication includes a series of processes that produce numerous identical integrated circuits in a semiconductor workpiece, e.g., a silicon wafer, in accordance with a circuit design. One important process is plasma etching, which is a process of transferring a pattern in a layer of mask material into another layer under the mask, such as a layer of conductive or dielectric material, by removing the layered material from the wafer surface.

Plasma etching is performed in a plasma reactor as depicted in Figure 1. Reactor 100 comprises a chamber 110 having a sidewall 112, a bottom 114, and a ceiling 160. Chamber 110 includes a process zone 118 in the middle, encompassing a volume of about 5,000 to about 50,000 cm³. Reactor 100 further comprises a process gas supply 120 that provides gases into chamber 110 through a gas manifold 162 and a gas distribution plate or showerhead 164, at ceiling 160 of chamber 110. Process exhausts, e.g., spent process gases and etch products, are pumped out of chamber 110 by a pump 140. A throttle valve 145 controls the pressure in chamber 110. Electrically grounded sidewall 112, bottom 114, ceiling 160, and showerhead 164 are usually made of aluminum with anodized aluminum coating on at least the interior surface of chamber 110. Chamber 110 further includes a pedestal 130 that supports a semiconductor wafer 190. Pedestal 130 is electrically isolated from bottom 114 by a supporting insulator 132 and is connected to a radio frequency (RF) power system 150 through a RF match network 155.

A control system 180 comprises a CPU 182, a memory 184, and support circuits 186. CPU 182 is coupled to the various components of reactor 100 to operate them. Memory 184 can be any computer-readable medium, such as random access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote to reactor

100 or CPU 182. A software routine or a series of program instructions stored in memory 184, when executed by CPU 182, causes reactor 100 to perform the desired process.

When plasma reactor 100 is used to etch a layer of material on wafer 150, chamber 110 is first evacuated by pump 140 to a pressure of less than about 1 mTorr. The wafer is typically transferred into chamber 110 from a load lock transfer chamber (not shown) maintained at near vacuum, and is placed on pedestal 130. The wafer can be held in place during the dielectric etching process by a mechanical or electrostatic chuck (not shown). There are grooves on the surface of pedestal 130, in which a coolant gas, such as helium, is circulated to control the temperature of the wafer.

Gaseous components are then released into chamber 110 at various volumetric flow rates to form a process gas. Once the pressure in chamber 110 is stabilized at a desired level, RF power system 150 is turned on to energize the process gas and form a plasma sheath in the process zone. RF match network 155 may also be tuned for efficient coupling between RF power system 150 and the plasma in processing chamber 110. The plasma density, defined as the number of ions per unit volume, may be enhanced by placing a plurality of magnets 170 around chamber sidewall 112 to provide a slowly rotating magnetic field inside the chamber 110. The magnets may be electromagnets driven with respective phases of a low frequency (e.g., 0.1-0.5 Hertz) AC current source (not shown). Alternatively, the magnets may be permanent magnets mounted on a supporting structure (not shown) rotating at, for example, 0.1-0.5 revolutions per second.

With pedestal 130 acting as a cathode electrode, grounded sidewall 112, ceiling 160 and showerhead 164 together serving as an anode electrode, the RF power system generates a negative voltage in process zone 118. A substantial DC bias thus exists between the plasma and the wafer, resulting in energetic ion bombardment on the wafer, which etches out unwanted portions on the wafer surface. When etching is complete, the plasma of the process gas is turned off after shutting down the RF power system 150.

To have a productive and reliable plasma chamber, there are many practical issues that need to be tackled, one of which is how to maintain a uniform plasma etch rate across the wafer surface. Etch rate refers to the rate at which a layered material is removed from a wafer surface, which is an important parameter for evaluating the performance of an etch process. A uniform etch rate across the entire wafer is desirable because many identical integrated circuits are formed simultaneously and it is critical to make sure they are all fabricated through identical

processes. It is relatively easy to have a uniform etch rate close to the wafer center, but more challenging near the wafer perimeter because the sudden interruption of wafer surface at the wafer edge adversely affects plasma energy distribution. Such edge effect on etch rate becomes more critical with the increase of wafer dimension and the reduction in the integrated circuit's

5 minimum feature size.

A conventional remedy for edge effects is to install a circular process kit 195 surrounding wafer 190 in chamber 110. Figure 2 provides more details about a process kit 220 and its position relative to a wafer 210. Dash lines 221, 223, 225 and 227 together define the top surface of a conventional process kit 220 prior to any erosion. Such surface contour can shape 10 the plasma field and ensure a uniform etch rate near the wafer edge. For instance, upper surface 225 forms an obtuse angle with the wafer surface, this angle being from 120° to 135°. Because of this angular orientation, plasma ions bombarding the surface 225 vertically will be deflected laterally toward the center of the wafer and scatter over a broader area above the wafer, rather than being concentrated at the edge of the wafer.

15 However, the top surface of process kit 220, when exposed to some kinds of etch chemistry, may react with the etchant and become eroded after a period of time. For example, a process kit made of quartz, a crystal form of silicon dioxide (SiO_2), is very reactive when it is exposed to a fluorocarbon-based plasma, e.g., CF_4 . The reaction of CF_4 with SiO_2 forms etch products SiF_4 , CO , CO_2 , and COF_2 , etc.

20 The erosion of the process kit not only generates a large amount of particulate contamination, but also destroys the spatial uniformity of etch rate near the wafer perimeter, resulting in more product defects. Solid curve 229 represents the receded contour of the conventional process kit 220 caused by the progressive erosion. As will be apparent, the eroded surface 229 has lost its particular angular effect on plasma ion redistribution.

25 Therefore, while the conventional process kit has proven effective in preserving the spatial uniformity of etch rate near the wafer perimeter, it is desirable to reduce the erosion occurring to the top surface of the process kit and prolong its lifetime.

SUMMARY OF THE INVENTION

The present invention is especially useful in oxide etch processes and other plasma-assisted semiconductor fabrication processes which are highly reactive with dielectric materials.

In a first aspect of the present invention, a portion of the top surface of the process kit is covered with a layer of fluorocarbon-based polymer. Since the polymer material is fluorocarbon-based, it is less likely to be affected by the fluorocarbon-based plasma. Therefore, this layer effectively insulates the process kit from erosion by the reactive species in the plasma
5 and substantially prolongs the lifetime of the process kit.

In a second aspect of the invention, the polymer material is made such that its permittivity is similar to that of the process kit. Such arrangement is preferred to maintain the spatial uniformity of the plasma property near the wafer edge during the fabrication process.

In a third aspect of the invention, the layer of fluorocarbon-based polymer is controlled to
10 be thin, e.g., 1.5 mm, so as to minimize the impact of the Coefficient of the Thermal Expansion (CTE) difference between the polymer material and the process kit. Even though CTE of the polymer material is significantly different from that of the process kit, its limited thickness minimizes the effect of temperature variation on the polymer layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Additional objects and features of the invention will be more readily apparent from the following detailed description and appended claims when taken in conjunction with the drawings, in which:

5 Figure 1 is a schematic view of a prior art magnetic-enhanced plasma reactor to practice a dielectric etching process;

Figure 2 is a sectional view of a portion of a prior art process kit before and after progressive erosion;

10 Figure 3 is a sectional view of a prior art process kit that has no particular protection against plasma erosion; and

Figure 4 is a sectional view of a process kit in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

The process kit of the present invention provides a uniform plasma ion and plasma energy distribution across the top surface of a semiconductor wafer. The process kit of the present invention resists erosion caused by the highly reactive species in the plasma and thereby significantly prolongs its lifetime to achieve higher production throughput and lower production consumable cost. The process kit of the present invention can be deployed in a plasma reactor, such as, for example, the Dielectric Etch eMAX System, the Dielectric Etch Super eCentura System, or the Centura MxP Dielectric Etch system, all of which are commercially available from Applied Materials Inc., Santa Clara, Calif.

Figure 3 provides a sectional view of pedestal 130, wafer 190, and conventional process kit 195 of Figure 1 with more details. Wafer 190 is secured at the center of the pedestal by an electrostatic chuck (not shown), or e-chuck. The e-chuck is supported by a dielectric member 390 having a cathode electrode 350 embedded therein. Cathode electrode RF power source 150 generates a negative voltage on cathode electrode 350 relative to an anode electrode at the ceiling of the chamber (not shown). A dielectric cylinder 360 and a supporting insulator 370 protect dielectric member 390 and other components inside the insulator 370 against corrosion. Wafer 190 is surrounded by a process kit 195, which is essentially a ring of a specific shape described below. Process kit 195 further comprises an inner ring 340 and an outer ring 330.

The axial thickness of process kit 195 varies radially such that inner ring 340 is thinner than outer ring 330. The top surface of process kit 195 is similar to that shown in Figure 2. Such specific thickness arrangement of process kit 195 performs two functions. First, thick outer ring 330 provides high electrical impedance to RF power coupling between the region near the edge of cathode electrode 350 and the anode electrode at the ceiling. A relatively high RF impedance can reduce plasma ion flux reaching the portion of cathode electrode 350 below outer ring 330, thereby confining the plasma energy right above the wafer and achieving a higher plasma etch rate. Second, thin inner ring 340 provides low RF impedance that promotes an ion flux from the plasma to the portion of the cathode electrode between the outer ring 330 and the wafer edge. Furthermore, the top surfaces of inner ring 340 and wafer 190 are maintained at the same level. As a result, thin inner ring 340 extends the plasma sheath (not shown) radially outward beyond the perimeter of wafer 310, thereby reducing the variation of the plasma sheath near the perimeter.

A significant issue with the usage of process kit 195 is that the process kit material can be progressively eroded depending on the chemical property of the plasma in the chamber. Since the dimension and shape of the process kit affect the plasma energy distribution near the wafer edge, such erosion inevitably changes the characteristics such as the etch rate of the etching process performed in the chamber. When such change accumulates to a certain degree, it will adversely affect the product quality. In addition, the particles generated by the erosion may deposit on the wafer surface, causing product defects. Such erosion is more significant with inner ring 340 because the plasma energy is more intense there than at outer ring 330.

In one embodiment of the present invention shown in Figure 4, the top surface of a process kit 420 is covered with a thin layer 425 of fluorocarbon-based polymer material, such as Polytetrafluoroethylene (PTFE).

This process kit has several advantages over the conventional process kit. First, the polymer material, which is inert when exposed in a fluorocarbon-based plasma environment, can serve as a satisfactory insulator in dielectric layer etching, preventing chemical reaction occurring at the top surface of the process kit. Second, the polymer material has similar permittivity, or dielectric constant, as the material comprising the dielectric layer on the wafer surface. A uniform distribution of permittivity from wafer surface to process kit top surface helps preserve a uniform distribution of plasma energy from wafer surface to process kit top surface. Otherwise, a sudden permittivity variation from the dielectric layer to the polymer

material could cause a dramatic change in etch rate near the wafer perimeter. Third, the polymer layer can also endure the plasma ion bombardment and temperature variation cycle in the chamber for a long period of time and thereby prolong the lifetime of the process kit. In addition, the process kit can be reused by re-coating the polymer layer over the top surface of the

5 process kit.

Even though the fluorocarbon-based polymer material has preferred chemical and dielectric properties, its thermomechanical property might pose one critical challenge for the proposed usage. More specifically, such material usually has very high coefficient of thermal expansion (CTE), e.g., 50-200 PPM/ $^{\circ}$ C. In contrast, the CTE of quartz is very low, usually
10 below 5 PPM/ $^{\circ}$ C. As a result, during a temperature change, the thermal deformation of the polymer layer is much higher than that of the quartz; and the polymer layer may be distorted and peel off during thermal expansion and contraction. An effective method of reducing the impact of CTE difference is to limit the thickness of the polymer layer. On the other hand, if the
15 polymer layer is too thin, it can not insulate the process kit from the plasma and sustain the plasma ion bombardment effectively. In one embodiment, the thickness of the polymer layer is less than 1.5 mm so as to avoid CTE difference impact and provide optimal erosion-resistant effect. The thickness of layer 425 shown in Figure 4 has been exaggerated relative to the thickness of wafer 410 and process kit 420.

The lifetime of a process kit is measured by the number of hours it has been exposed to
20 radio frequency (RF) signals in a plasma etching environment. Such exposure is referred to as RF hours. The RF hours of a process kit in accordance with the present invention can be 500-600 RF hours in a mild plasma environment, compared with 150 RF hours of a conventional process kit without the fluorocarbon-based coating.

Different manufacturing techniques are available for producing the fluorocarbon-based
25 layer on the top surface of the process kit. When the polymer layer is relatively thin, e.g., 0.5 mm, a technique such as sputtering can be used to deposit the material on the top surface of a process kit. If the layer is relatively thick, a technique such as thermal coating can be used to create the layer on the top surface of a process kit.

The foregoing description, for purposes of explanation, uses specific nomenclature to
30 provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. The embodiment is chosen and described in order to best explain the principles of the invention and

its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. Thus, the foregoing disclosure is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in view
5 of the above teachings.

It is intended that the scope of the invention be defined by the following claims and their equivalents.